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Path-Decoupled Cation-Eutaxy III–V van der Waals Memristive Semiconductors for Mitigating the Neuromorphic Accuracy-Energy Trade-off

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ABSTRACT

Transistor-based computing faces a fundamental energy-resolution trade-off: lowering the conductance reduces the programming energy (Eprog) but simultaneously narrows the dynamic range (G_{max}/G_{min}) required for multilevel state discrimination. A memristor offers analog programmability, but it suffers from the same limitation because reducing the conductance decreases G_{max}/G_{min}, degrading the learning accuracy. Here, a path-decoupled III–V van der Waals (vdW) memtransistor overcomes this constraint via the spatial separation of the ionic and electronic transport pathways. Using $H_xK_{1-x}GaSb_2$, K^+ vacancies confined to the vdW gap serve as mobile ionic species, while holes conduct within the covalently bonded [$GaSb_2$] layers. This decoupling yields a high K^+ diffusivity and enables memristive switching at markedly reduced voltages. The memristive window G_{max}/G_{min}—which is set by ionic motion—remains invariant under gate modulation, whereas E_{prog} decreases via electrostatic control of the channel conductance. Consequently, the synaptic plasticity and neuromorphic inference maintain a high accuracy (>80%), while E_{prog} is reduced by more than an order of magnitude. The results establish ionic-electronic path decoupling as a general strategy for breaking the accuracy-energy trade-off in emerging neuromorphic hardware and position III–V vdW materials, which are promising candidates for application in low-energy, artificial intelligence accelerators.

1 | Introduction

The rapid increases in artificial intelligence workloads have intensified the need for hardware with capacity for energy-efficient computation [1–3]. However, transistor-based digital systems inherently struggle to scale energy consumption because multilevel programming introduces a fundamental conflict between the programming energy (E_{prog}) and state resolution [4–6]. When a fixed drain-source voltage V is applied, increasing the channel resistance R reduces the current $I = V/R$ and power

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consumption $P = V^2/R$ [7, 8]. However, this simultaneously enlarges the resistance-capacitance delay $\tau = RC$, limiting the sensing margin and degrading the levels of distinguishability of the multilevel states. Conversely, reducing R enhances the state resolution but inevitably increases P. This energy-resolution trade-off fundamentally constrains further scaling in transistor-based hardware.

Neuromorphic computing offers an alternative route via the implementation of analog state variables for in-memory computation [9–11]. Memristors are widely studied as artificial synapses because conductance can be incrementally modified with a low E_{prog} [12–14]. Nevertheless, reducing the energy consumption requires operating memristors in the low conductance regime, which narrows the dynamic range G_{max}/G_{min} (the ratio of the maximum and minimum synaptic conductances), thereby diminishing the weight resolution and degrading the learning accuracy [15–17]. Hence, realizing a large G_{max}/G_{min} requires stronger programming pulses to induce larger changes in resistance, which increases E_{prog}—resulting in a trade-off between G_{max}/G_{min} and energy consumption [18–20].

Memtransistors combine ion-migration-driven memristive switching with electrostatic gating in a three-terminal configuration, enabling the potential for tuning E_{prog} through electrostatic modulation of the channel conductance, independently from the memristive conductance window [21]. A programming pulse applied across the channel ($V_{D,pulse}$) sets the ion configuration that defines G_{max}/G_{min}, whereas a gate voltage V_G modulates the carrier density and current flow via electrostatic control. In principle, this separation should enable the maintenance of a wide G_{max}/G_{min} while reducing E_{prog}. However, current implementations—including monolayer MoS_2 memtransistors [22]—face limitations: (i) the tortuous ion-migration pathways caused by randomly oriented grain boundaries increase the diffusion barrier [23, 24], leading to high programming voltages; and (ii) the ionic and electronic transport pathways are not spatially decoupled, causing carrier scattering [25] and increasing the energies required for ion motion and charge transport. Moreover, the G_{max}/G_{min} behavior under gate modulation has not been established, leaving the energy-G_{max}/G_{min} relationship unresolved.

Realizing a memtransistor that simultaneously supports a wide G_{max}/G_{min}, high gate tunability, and low E_{prog} requires materials that (1) host mobile charged species with stable levels of diffusion under electric fields, (2) provide low-barrier migration pathways to ensure high diffusivities, and (3) preserve semiconducting electronic transport within channels structurally decoupled from the ionic migration pathways. III–V layered semiconductors containing mobile ions within van der Waals (vdW) gaps satisfy many of these criteria [26], yet their suitabilities for neuromorphic operation—particularly in maintaining high learning accuracies at low energies—remain insufficiently explored.

Here, we reveal that a path-decoupled III–V vdW memtransistor can overcome the trade-off between G_{max}/G_{min} and energy. Using $H_xK_{1-x}GaSb_2$ as a representative system, we employ K^+ vacancies generated via a topochemical reaction [27] as mobile ionic species confined to the vdW gap, while hole transport occurs in the semiconducting [$GaSb_2$] layers. This structural decoupling results in a high ionic diffusivity, and it enables memristive switching with gate tunability at a substantially reduced operating voltage compared to that of grain boundary-mediated systems. Using two- and three-terminal configurations, we emulate synaptic plasticity and confirm that gate control suppresses E_{prog} without compromising G_{max}/G_{min}. Finally, we demonstrate low-energy neuromorphic inference while maintaining a recognition accuracy of >80%, establishing ionic-electronic path decoupling as a viable strategy to break the accuracy-energy trade-off that constrains current resistive random-access memory (RRAM) technologies.

2 | Results and Discussion

2.1 | Path-Decoupled Ion and Carrier Transport Within the III–V vdW Memtransistor

Figure 1a shows the three-terminal III–V vdW memtransistor, wherein a III–V layered semiconductor serves as the electronic channel. Under an applied drain-source bias V_D, holes drift within the III–V layers, whereas K^+ ions migrate through the vdW gap. A SiO_2/p^{++}-Si back-gate underneath the channel modulates the hole density via V_G, enabling electrostatic control of the channel conductance. Crucially, the ionic and electronic transport pathways are spatially separated (Figure 1b): the ionic flux $\boldsymbol{J}_\mathbf{i}$ arises within the vdW gap, and the hole flux $\boldsymbol{J}_\mathbf{q}$ flows within the covalently bonded III–V layers. Under a positive V_D, K^+ ions drift along the vdW gap, leaving K vacancies V_K' that accumulate at the opposite metal/semiconductor interface. The local vacancy accumulation enhances p-type doping, resulting in a reduction in the Schottky barrier height and thus facilitating hole injection from the metal (Figure S1).

The coupled hole-ion transport can be described using a linear flux-force relation (Figure 1c) [28, 29]:

$$\begin{bmatrix} J_\mathbf{i} \\ J_\mathbf{q} \end{bmatrix} = \begin{bmatrix} L_{ii} & L_{iq} \\ L_{qi} & L_{qq} \end{bmatrix} \begin{bmatrix} X_\mathbf{i} \\ X_\mathbf{q} \end{bmatrix} \tag{1}$$

Here, L_{ii} , L_{qq} , L_{iq} , and L_{qi} represent the ionic diffusivity, electronic conductivity, field-driven ion-response coefficient, and ion-hole coupling coefficient reflecting the doping-induced modulation of the Schottky barrier, respectively. The generalized forces $\boldsymbol{X}_\mathbf{i}$ and $\boldsymbol{X}_\mathbf{q}$ correspond to the chemical-potential gradient and electric field, respectively.

2.1.1 | Field-Driven Ionic Migration (L_{iq})

Figure 1d shows field-driven ion transport. $\boldsymbol{J}_\mathbf{i}$ follows the Nernst-Planck relation ($\boldsymbol{J}_\mathbf{i} = -D_i\partial C_i/\partial x + \mu_i C_i \boldsymbol{E}$) [30, 31], where D_i, C_i, μ_i, and $\boldsymbol{E}$ represent the ion diffusivity, concentration, mobility, and electric field, respectively. In the drift regime with $\mu = Z_i e D_i/kT$ (Note S1), this becomes

$$J_\mathbf{i} \approx \frac{C_i Z_i e D_i}{kT} E \tag{2}$$

Thus,

$$L_{iq} \approx \frac{C_i Z_i e D_i}{kT} \tag{3}$$

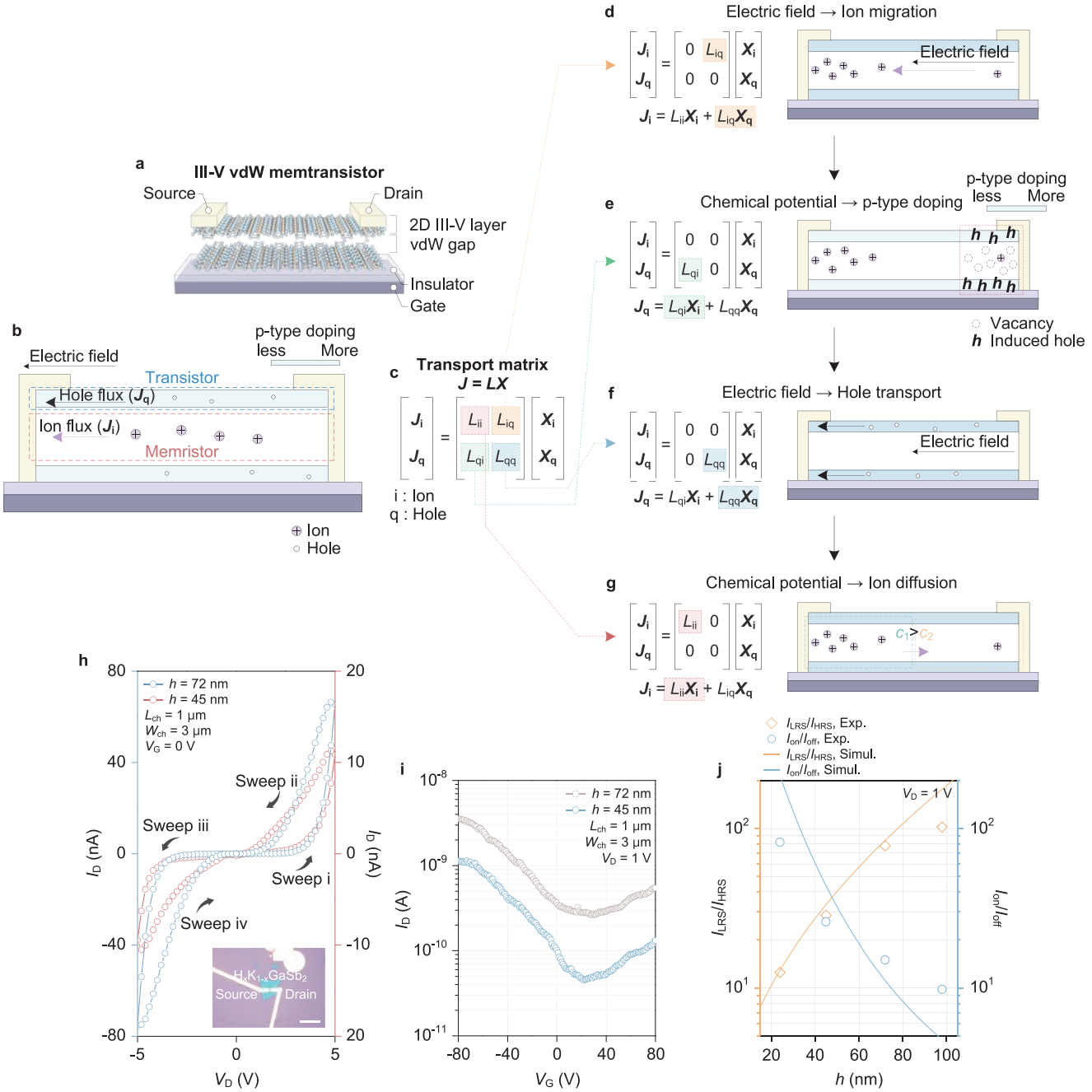

FIGURE 1 | Matrix-formulated, path-decoupled operation of a III–V vdW memtransistor. a) Device architecture of a three-terminal III–V vdW memtransistor. b) Spatially decoupled transport paths for holes and ions within the III–V vdW memtransistor. A lateral electric field drives $\boldsymbol{J_q}$ in the 2D III–V layer (transistor path) and $\boldsymbol{J_i}$ in the vdW gap (memristor path), leading to an asymmetric p-type doping profile within the III–V channel. c) Path-decoupled ionic-electronic transport written in matrix form. $\boldsymbol{X_q}$ and $\boldsymbol{X_i}$ denote the thermodynamic driving forces associated with the electric field and chemical potential, respectively. L_{iq}, L_{qi}, L_{qq}, and L_{ii} represent the field-to-ion transport coefficient, ion-state-to-carrier-conduction coupling coefficient affecting doping/barrier modulation, electronic conductivity, and ionic diffusivity, respectively. d) Electric field-driven ion transport (L_{iq}). Ions migrate laterally within the vdW gap under an applied electric field, leading to an asymmetric ionic/vacancy profile. e) Resistance-state transition induced by ion transport-driven p-type doping and Schottky barrier modulation (L_{qi}). The local accumulated vacancy concentration modifies the hole density within the III–V channel, leading to a change in the Schottky barrier height. f) Electric field-driven carrier transport (L_{qq}). g) Relaxation via chemical-potential-driven ionic diffusion (L_{ii}). h) Hysteresis I_D–V_D curves indicating a counterclockwise hysteresis (sweeps i–iv) at $V_G = 0$ V. $L_{ch} = 1$ μm and $W_{ch} = 3$ μm. Forward and reverse V_D sweeps of the devices with thicknesses of 45 and 72 nm produce counterclockwise I_D–V_D loops. An optical micrograph of an $H_xK_{1-x}GaSb_2$ memtransistor is shown in the inset. i) Transfer characteristics (I_D–V_G) of the devices with thicknesses of 45 and 72 nm at $V_D = 1$ V. $L_{ch} = 1$ μm and $W_{ch} = 3$ μm. j) Thickness-dependent I_{LRS}/I_{HRS} and I_{on}/I_{off}. The extracted I_{LRS}/I_{HRS} and I_{on}/I_{off} values reveal trends consistent with those of their respective analytical models.

2.1.2 | Ion-Induced Schottky Barrier Modulation (L_{qi})

Figure 1e shows the effect of vacancy accumulation on the Schottky barrier. The doping-induced barrier reduction $\Delta\Phi_{dop}$ is governed by the image-force lowering mechanism [7, 22, 32] and scales with the square root of the dopant density p and the width w (Note S2):

$$\Delta\Phi_{dop} \propto \sqrt{pw} \tag{4}$$

Thus, increasing V_K' accumulation enhances local p-type doping and decreases the Schottky barrier height, thereby increasing hole injection ($\boldsymbol{J_q} = L_{qi}\boldsymbol{X_i} + L_{qq}\boldsymbol{X_q}$). This ion-induced modulation of the barrier underlies the memristive switching.

2.1.3 | Gate-Dependent Hole Transport (L_{qq})

Figure 1f depicts hole transport within the III–V channel under V_D. The coefficient L_{qq} corresponds to the channel conductivity, which depends on gate-induced changes in the hole concentration, mobility and barrier height, and thus, electrostatic gating directly modulates $\boldsymbol{J_q}$ via the $L_{qq}\boldsymbol{X_q}$ term [33, 34].

2.1.4 | Diffusion-Driven Ionic Relaxation (L_{ii})

After removing the external $\boldsymbol{E}$, the ions relax toward equilibrium via chemical-potential-driven diffusion (Figure 1g), as described by $\boldsymbol{J_i} = -D_i\partial C_i/\partial x$ [31, 35], and thus, $L_{ii} \equiv D_i$, which governs the retention behavior.

Combined, this framework describes the sequential processes within the III–V vdW memtransistor: electric field-driven ion migration (L_{iq}), ion-induced Schottky barrier modulation (L_{qi}), gate-controlled hole transport (L_{qq}), and post-bias ionic relaxation (L_{ii}). Within this framework, these coefficients can be qualitatively related to experimentally measurable quantities (Note S3).

We fabricated three-terminal devices using $H_xK_{1-x}GaSb_2$, with an enlarged interlayer spacing that facilitated ion migration, to validate this transport model. Channel thickness corresponds to the thickness of the exfoliated nanosheet and reflects the number of stacked vdW layers (Figure S2). Au (100 nm, work function: 5.1 eV) was deposited to form Schottky contacts, enabling the direct observation of barrier modulation.

The devices exhibit clear memristive hysteresis in the current–voltage (I_D–V_D) curves under positive and negative biases (Figure 1h). Sweeping from 0 → 5 V switches the device from a high-resistance state (HRS) to a low-resistance state (LRS), and the LRS persists as the bias returns (5 → 0 V). Reversing the polarity switches LRS → HRS at a low bias and sweeping to –5 V drives the HRS → LRS transition again. The HRS → LRS transition corresponds to vacancy accumulation that lowers the Schottky barrier, increasing hole injection—consistent with the $L_{qi}\boldsymbol{X_i}$ term—whereas the reverse sweep restores the barrier height (Note S2). The memristive switching behavior is maintained during repeated cycling (Figure S3), and the switching voltage also exhibits small cycle-to-cycle variation across different devices (Figure S4), consistent with the reliable ion-migration pathway within the vdW gaps. In addition, the separated LRS and HRS are retained for 3600 s (Figure S5).

The transfer characteristics (Figure 1i) reveal p-type behavior: sweeping V_G from –80 to 80 V decreases I_D, reflecting the gate dependence of L_{qq}. The memtransistor behavior is confirmed by the coexistence of I_D–V_D hysteresis and gate-tunable conductance (Figure S6). Owing to the spatial separation of the ion and hole paths, K^+ ions migrate through the vdW gap with low activation energy, enabling memristive switching at ±5 V—which is lower than that of grain boundary-mediated devices.

Remarkably, the LRS-to-HRS current ratio (I_{LRS}/I_{HRS}) increases with channel thickness h: 28.5 (45 nm) and 77.9 (72 nm, Figure 1h). As reverse-biased Schottky transport is governed by thermionic emission, the I_{LRS}/I_{HRS} reflects the difference in effective barrier height. $\Delta\Phi_{dop}$ increases with thickness due to the larger total mobile ion population, which enhances image-force lowering. Thus, $\Delta\Phi_{dop}$ depends on $h^{1/2}$ (Note S4), yielding a stretched-exponential dependence for I_{LRS}/I_{HRS}. Devices with thicknesses from 24 to 98 nm exhibit ratios ranging from 12.5 to 102, which is consistent with the analytical model (Figure 1j; Figure S7).

In contrast, the transistor on/off ratio (I_{on}/I_{off}) decreases with thickness—from 26 → 15 (45 nm → 72 nm) and 82 → 9.8 (24 nm → 98 nm, Figure 1j and Figure S8)—indicating the partial screening of the gate field by mobile ions. This behavior parallels the gate-field screening reported in perovskites [36, 37]. As ions mainly move within the vdW gap (with minimal vertical displacements), we adopt an ion-induced Debye screening model: $\lambda_D{}^2 = \varepsilon k\ T/q^2N_{ion}$ [38], where λ_D is the Debye length (Note S5). The gate potential decays exponentially along the thickness direction as $\exp(-h/\lambda_D)$, and modeling I_{on}/I_{off} with this screening factor reproduces the experimentally observed thickness dependence (Figure 1j).

Thus, increasing the thickness enhances the ion-driven barrier modulation (L_{qi}) but weakens the electrostatic gating (L_{qq}), revealing a thickness-dependent trade-off between memristor and transistor characteristics. The contrasting thickness dependences of L_{qi} and L_{qq} directly support the spatial separation of ionic and hole transport within the vdW gap and III–V layers, respectively.

2.2 | vdW Gap-Enabled High K^+ Ion Diffusivity

The spatial decoupling of the ionic and electronic transport pathways is a key structural feature that enables the III–V vdW memtransistor to operate under extremely small electrical driving forces. We analyzed the material structure and corresponding transport mechanisms to clarify the origin of its low-energy operation (Figure 2a). In the vdW architecture, the electronic (III–V channel) and ionic (vdW gap) pathways are physically separated, and thus, the electronic current I_e and ionic current I_i are spatially independent. This separation suppresses ion-induced carrier scattering within the channel, ensuring efficient hole transport, whereas the vdW gap provides a low-barrier, linear diffusion pathway for K^+ ions. As a result, resistance-state transitions occur rapidly, even at low applied voltages.

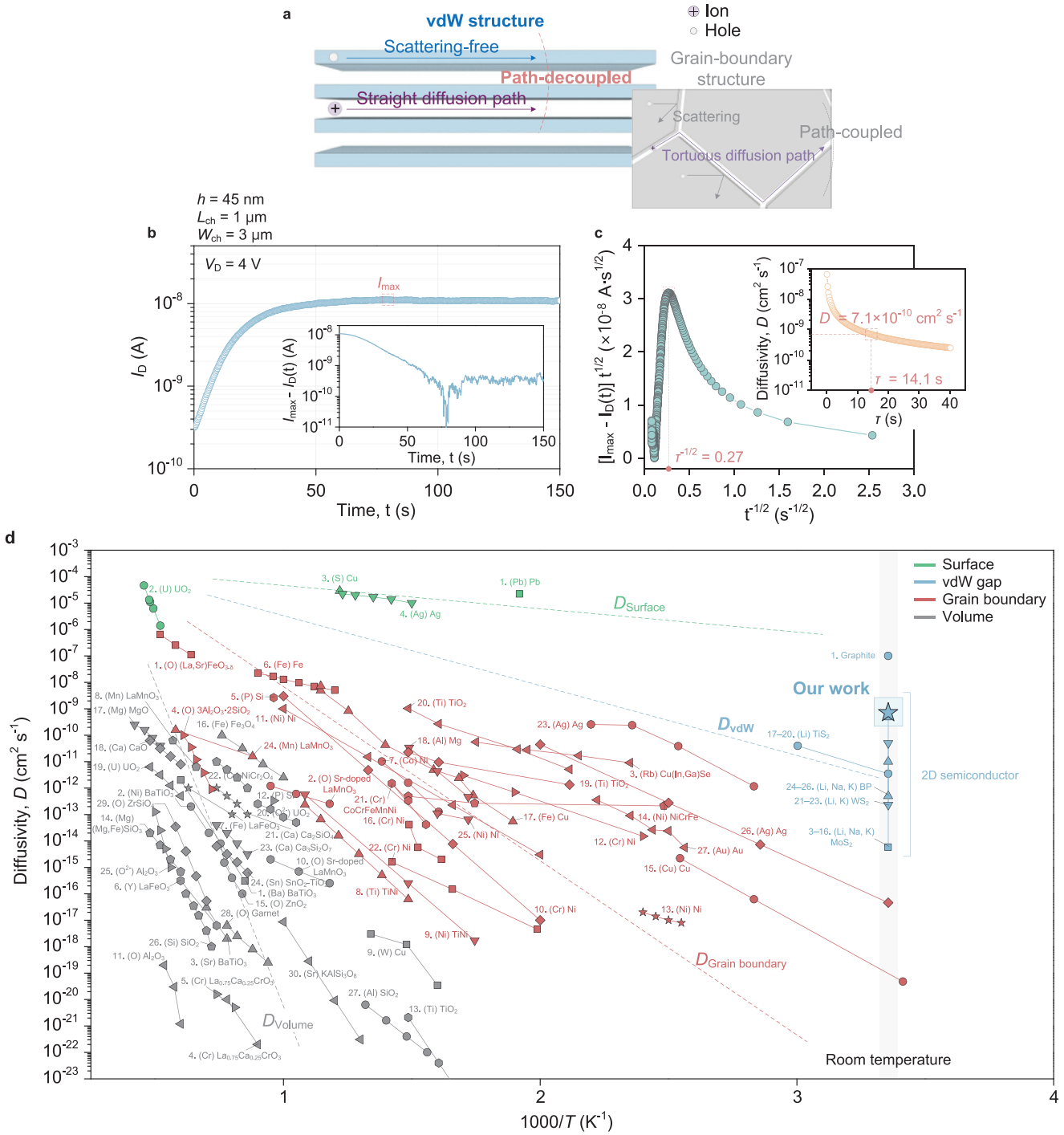

FIGURE 2 | Fast K^+ ion diffusion within the vdW gap enabled by the path-decoupled structure. a) Path-decoupled ionic-electronic transport within the $H_xK_{1-x}GaSb_2$ vdW structure. The K^+ ions migrate within a straight, relatively scattering-free vdW gap that is spatially separated from the hole transport channel, thus decoupling the ionic and electronic paths. The inset shows spatially coupled ionic-electronic transport within a grain-boundary structure. Mobile ions and electronic carriers follow tortuous grain-boundary networks, and thus, the ionic and electronic paths are spatially coupled, and the grain boundaries induce carrier scattering. b) Chronoamperometry under constant $V_D = 4$ V. I_D increases transiently toward I_{max}. The inset shows $I_{max} - I_D(t)$ against time, which is used to extract D. c) Cottrell-type extraction of D. The peak in $[I_{max} - I_D(t)]t^{1/2}$ defines the characteristic time τ. This characteristic time, using L_{ch} and the relation $D \approx {L_{ch}}^2/\tau$, provides a device-level estimate of D. The inset shows the plot of $[I_{max} - I_D(t)]t^{1/2}$ against $t^{-1/2}$ used to determine ${t^{-1/2}}_{peak} = \tau^{-1/2}$. d) Comparison of D values across transport pathways. The D of the $H_xK_{1-x}GaSb_2$ device is plotted with the reported D values along different diffusion pathways, including the surface, vdW gap, grain boundaries, and volume. The measured D lies among those of the diffusion pathways ($D_{Surface} > D_{vdW} > D_{Grain\ boundary} > D_{Volume}$), and it exceeds most grain boundary and bulk values, yet it is lower than that of typical surface diffusion. In 2D semiconductors, $H_xK_{1-x}GaSb_2$ exhibits a high D, highlighting the efficient ionic transport realizable through vdW gap channels. The numeric labels denote the index of each material, with the corresponding materials provided in Tables S1–S4.

We performed chronoamperometry under a constant drain bias and applied memristor-based Cottrell analysis [39] to quantify the diffusivity D within $H_xK_{1-x}GaSb_2$ (Figure 2b,c). Upon applying V_D = 4 V, $I_D(t)$ gradually increases from an initial value to its steady-state maximum I_{max} (Figure 2b and inset), reflecting the progressive migration of K^+ ions within the vdW gap and the corresponding modulation of the device resistance. We assume that the rate of increase in I_D in this regime is governed by the K^+ ion transport kinetics. Following the Cottrell relation, $I_{max} - I_D(t) = B(D/t)^{1/2}$, where B is a constant, and $[I_{max} - I_D(t)]t^{1/2}$ scales with $D^{1/2}$ (Note S6). Immediately after bias application, limited ion displacement yields a small $[I_{max} - I_D(t)]t^{1/2}$, and $I_D(t) \approx I_{max}$ at extended times, again reducing the value. Hence, the peak in the $[I_{max} - I_D(t)]t^{1/2}$–$t^{-1/2}$ plot corresponds to the characteristic ionic-transit time (Figure 2c). We define this peak time as τ, which is the representative time for K^+ ions to traverse the channel length L_{ch}, and obtain τ = 14.1 s. Using the diffusion time relation $\tau = {L_{ch}}^2/D$, we extract a D of 7.1×10^{-10} cm^2 s^{-1} (inset, Figure 2c). Applying the same Cottrell analysis to the device with L_{ch} = 200 nm yields a reduced characteristic time of τ = 0.60 s, while the diffusivity remains nearly unchanged at $D = 6.36 \times 10^{-10}$ cm^2 s^{-1}, comparable to that of the L_{ch} = 1 μm device (Figure S9). In contrast, increasing the temperature to 373 K in the L_{ch} = 1 μm device decreases τ to 2.97 s while increasing the diffusivity to D = 3.3×10^{-9} cm^2 s^{-1} (Figure S10). These results indicate that both channel-length scaling and temperature increase reduce the ion redistribution time; however, the former operates by shortening the redistribution length scale, whereas the latter arises from an increase in ionic diffusivity.

Figure 2d compares the extracted D to those of materials with various diffusion pathways to contextualize this value. In crystalline solids, diffusion generally follows $D_{Surface} > D_{Grain\ boundary} > D_{Volume}$, reflecting decreasing levels of pathway openness and increasing activation barriers [30]. We introduce the vdW gap as an additional diffusion pathway. As the vdW spacing provides an extended, low-barrier, structurally ordered route, its D satisfies

$$D_{Surface} > D_{vdW} > D_{Grainboundary} > D_{Volume}$$

The measured D exceeds those of typical volume- or grain boundary-mediated systems, and it is comparable to or larger than the values reported for other vdW-mediated ion conductors (full numerical comparison is shown in Tables S1–S4). These results confirm that the vdW gap within $H_xK_{1-x}GaSb_2$ provides a highly efficient ionic conduction pathway, enabling rapid K^+ ion migration and thus low-voltage memristive switching.

2.3 | Energy-Efficient Gate-Tunable Synaptic Plasticity

The fast K^+ ion diffusion within the vdW gap enables the continuous conductance modulation of the channel at low operating voltages, which is a key requirement in implementing energy-efficient synaptic devices [40, 41]. In biological neural systems, neuromodulatory afferents regulate neurotransmission between pre- and postsynaptic neurons by releasing neuromodulators, thus enabling heterosynaptic plasticity [42, 43]. We configured the three-terminal $H_xK_{1-x}GaSb_2$ memtransistor such that the drain, source, and gate corresponded to the pre- and postsynaptic neurons and neuromodulatory afferent, respectively, to emulate this behavior (Figure 3a). In this configuration, $V_{D,pulse}$ applied between the source and drain modulates the channel conductance and thus sets the synaptic weight, whereas the gate terminal provides an additional degree of freedom for conductance tuning.

We first applied positive (4 V) and negative (–4 V) $V_{D,pulse}$ values without a gate bias to demonstrate homosynaptic plasticity (Figure 3b). Upon applying each 4 V pulse, the postsynaptic conductance was measured at V_D = 2 V, which was repeated for 15 cycles, resulting in a gradual increase in conductance characteristic of long-term potentiation (LTP). Subsequently, repeating the same procedure with pulses of –4 V induces a progressive decrease in conductance, corresponding to long-term depression (LTD). G_{max}/G_{min} increases from 8.8 in the 24-nm-thick device to 47.9 in the 98-nm-thick device while remaining reproducible across multiple devices, consistent with the increasing I_{LRS}/I_{HRS} observed previously (Figure 1j, Figures S11–S13, Tables S5–S6). Even under repeated cycling, with 30 up-down pulse sweeps defined as one cycle and 17 cycles in total (510 pulses), the coefficient of variation (σ/μ, where σ and μ denote the standard deviation and mean of the G_{max}/G_{min}, respectively) of G_{max}/G_{min} remains as low as 0.09 (Figure 3c). This cycle-to-cycle uniformity and endurance arise from K^+ ion migration within the vdW gaps, which enables stable switching accompanied by reproducible pulse-to-pulse conductance updates (Figure S14). In addition, reducing the channel length and increasing the temperature decrease the pulse number required to reach conductance saturation during potentiation and depression (Figures S15 and S16). These results further indicate that homosynaptic potentiation and depression are governed by ion migration within the vdW gaps and can be robustly programmed by $V_{D,pulse}$ in the two-terminal configuration.

We applied the same $V_{D,pulse}$ amplitudes used in LTP and LTD (4 and –4 V, respectively) while sweeping V_G from –80 to 80 V to emulate heterosynaptic plasticity (Figure 3d). Modulating V_G shifts the initial conductance states of the LTP and LTD curves, enabling a wide conductance tunability. Distinct conductance states remain well separated for 500 s even under gate bias (Figure S17). Notably, G_{max}/G_{min} remains nearly constant over the entire V_G window, whereas the reduced conductance at high V_G results in a substantial decrease in E_{prog} from 110 to 9.8 pJ (Figure 3e); this trend is consistently reproduced across different devices (Figure S18 and Table S7). This behavior is observed because V_G only modulates the electronic flux term (L_{qq}) in the relation $\boldsymbol{J_q} = L_{qi}\boldsymbol{X_i} + L_{qq}\boldsymbol{X_q}$, whereas the ion-induced Schottky barrier modulation term (L_{qi}) affected by field-driven ion migration (L_{iq})—which determines G_{max}/G_{min}—remains unaffected. E_{prog} represents the electrical energy consumed during programming and governed by the gate-controlled drain current I_D (Experimental Section); because the device exhibits p-type characteristics, a positive V_G reduces L_{qq}, thereby reducing I_D and lowering E_{prog}. Crucially, unlike conventional memristors, wherein higher resistance states diminish their G_{max}/G_{min} values, our device maintains a large G_{max}/G_{min} while minimizing the energy consumption under a positive V_G.

We further compared the electric-field dependence of G_{max}/G_{min} (Figure 3f) and energy consumption (Figure 3g) to those of single-channel, grain boundary-mediated memtransistors. In

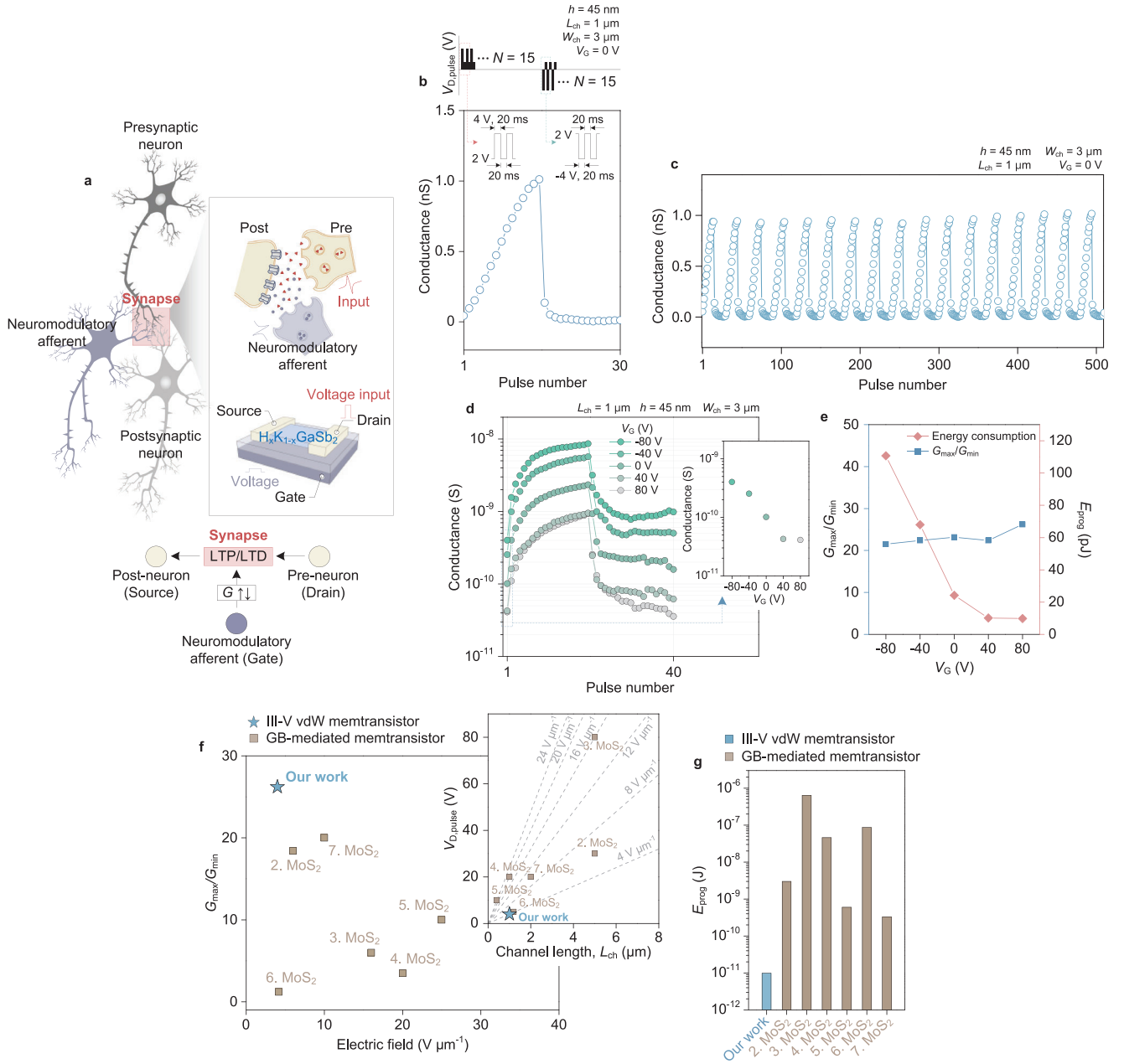

FIGURE 3 | Energy-efficient gate-tunable synaptic operation with a preserved G_{max}/G_{min}a) Schematic of heterosynaptic neuromodulation and its emulation using the $H_xK_{1-x}GaSb_2$ memtransistor. In the artificial synapse, the pre- and postsynaptic neurons and neuromodulatory afferent correspond to the drain, source, and gate terminals, respectively. LTP and LTD are induced by $V_{D,pulse}$, whereas V_G only changes the conductance (G), without altering the LTP/LTD characteristics. b) LTP and LTD of a 45-nm-thick device under consecutive stimulation of 15 excitatory and inhibitory pulses at $V_G = 0$ V. The pulse schemes are shown in the inset. $L_{ch} = 1$ μm and $W_{ch} = 3$ μm. c) Endurance of homosynaptic plasticity. Sequences of 15 LTP and LTD pulses (30 programming pulses) were repeated 17 times (510 pulses in total) without degradation. d) Gate control of the synaptic weight in a 45-nm-thick device varying V_G from −80 to 80 V in 40 V steps. Consecutive stimulation of 20 excitatory and inhibitory pulses is applied. The first postsynaptic conductance is shown as a function of V_G in the inset. $L_{ch} = 1$ μm and $W_{ch} = 3$ μm. e) Gate dependences of G_{max}/G_{min} and programming energy (E_{prog}). G_{max}/G_{min} remains almost constant across V_G, whereas the E_{prog} decreases as V_G increases. f) G_{max}/G_{min} against electric field. The $H_xK_{1-x}GaSb_2$ memtransistor exhibits a high G_{max}/G_{min}, even under the lowest electric field. $V_{D,pulse}$ as a function of L_{ch} for $H_xK_{1-x}GaSb_2$ and grain boundary-mediated memtransistors is shown in the inset. The $H_xK_{1-x}GaSb_2$ memtransistor operates at a lower $V_{D,pulse}$ than those of grain boundary-mediated memtransistors with comparable L_{ch} values. g) Levels of E_{prog} of the $H_xK_{1-x}GaSb_2$ and grain boundary-mediated memtransistors, indicating that the former is orders of magnitude lower.

such systems, the resistance-state transitions are governed by the quantities of ions or vacancies accumulating at their metal-semiconductor interfaces, and the resulting ion fluxes can be approximated by $\boldsymbol{J_i} \approx L_{iq}X_q = C_iZ_ieD_i\boldsymbol{E}/kT$ (Figure 1d). As a higher D_i enables a larger ionic displacement under the same $\boldsymbol{E}$, the vdW-gap-enabled high D_i facilitates resistance switching under lower $\boldsymbol{E}$. Our device exhibits stable LTP and LTD under a small electric field of $\boldsymbol{E}$ = 4 V μm^{-1} (calculated using $V_{D,pulse}$ = 4 V and L_{ch} = 1 μm), yielding the widest G_{max}/G_{min} of 26.2 among those of the compared devices (Figure 3f; Table S8). Moreover, the energy consumption of 9.8 pJ is orders of magnitude lower than that of grain boundary-mediated memtransistors (Experimental Section). Compared to typical metal-insulator-metal memristors, our device exhibits a relatively large G_{max}/G_{min} under lower operating fields while maintaining a low energy consumption with further device scaling expected to provide additional energy benefits (Figures S19 and S20). As electrostatic gating reduces L_{qq} but leaves L_{qi} unaffected, the wide G_{max}/G_{min} can be preserved while minimizing the energy cost, thus overcoming the trade-off between G_{max}/G_{min} and E_{prog} commonly observed in a memristive device.

2.4 | Accuracy-Energy-Decoupled Neuromorphic Learning

We performed simulations for handwritten-digit classification using the Modified National Institute of Standards and Technology (MNIST) dataset to evaluate the learning capacity and energy efficiency of our memtransistor-based artificial synapse [44]. Figure 4a shows the three-layer perceptron comprising input, hidden, and output layers with 400, 100, and 10 neurons corresponding to the digit classes 0–9, respectively. Each input neuron is directly mapped to one pixel of a 20 × 20 MNIST image. The input vector $\boldsymbol{x}$ is multiplied by the first synaptic weight matrix $\boldsymbol{W^{(1)}}$ and passed through an activation function to produce the hidden-layer output vector $\boldsymbol{y}$, which then serves as the input vector for the second synaptic weight matrix $\boldsymbol{W^{(2)}}$. After the second activation, the resulting output vector $\boldsymbol{z}$ represents the classification result. In this framework, each element of $\boldsymbol{W^{(1)}}$ and $\boldsymbol{W^{(2)}}$ corresponds to the conductance of an individual memtransistor within the respective crossbar array (400 × 100 and 100 × 10).

In the $H_xK_{1-x}GaSb_2$ memtransistor, K^+ ion migration within the vdW gap and the corresponding change in the Schottky barrier establishes the conductance window G_{max}/G_{min}, which determines the synaptic weight resolution and thus directly governs the recognition accuracy (Figure 4b) [45, 46]. As this process is set by the ion-induced Schottky barrier modulation L_{qi}, which is insensitive to electrostatic gating, G_{max}/G_{min} remains unchanged as V_G varies. In contrast, V_G only modulates the electronic conduction term L_{qq}, adjusting the overall channel conductance—and thus the energy consumption—without altering the changes in the ionic barrier that define G_{max}/G_{min} (Figure 4c). As a result, the accuracy (G_{max}/G_{min}) and energy (conductance) can be independently tuned. Conventional memristors lack this separation: realizing a large G_{max}/G_{min} requires a higher operating voltage, inherently linking an improved accuracy to an increased energy cost. The III–V vdW memtransistor overcomes this trade-off [20] via its spatially decoupled ion and hole pathways. The vdW gap provides a highly diffusive, low-barrier route for ion migration, enabling a large G_{max}/G_{min} at a low voltage, while electrostatic gating selectively lowers L_{qq} to reduce the energy consumption. Thus, the device realizes accuracy-energy decoupling, maintaining a high recognition accuracy while substantially lowering E_{prog}.

We evaluated the learning performance by implementing the experimentally extracted LTP/LTD characteristics from five different devices (Figures S12, S13, S18 and Tables S5–S7) within the simulation framework. As shown in Figure 4d, the device with h = 24 nm exhibits a degraded accuracy due to its limited G_{max}/G_{min}, whereas devices with $h \geq 45$ nm maintain high accuracies, regardless of further increases in h (Figure S21). We thus used the 45-nm-thick device as the representative configuration, as it supported a high accuracy and an efficient gate tunability. Simulations performed at V_G = −80, −40, 0, 40, and 80 V reveal that the recognition accuracy remains almost constant at 71.5 ± 0.8% (Figure 4e), consistent with the confusion matrices (Figure S22). This invariance is observed because ionic barrier modulation (L_{qi}) is minimally affected by electrostatic gating, thus maintaining G_{max}/G_{min} (Figure 3d). Meanwhile, the programming energy per image ($E_{p,image}$) [47, 48] decreases significantly at a positive V_G, because the device exhibits larger and smaller conductances at negative and positive V_G values, respectively. As V_G is swept from −80 to 80 V, $E_{p,image}$ decreases from 447 to 26.6 nJ (Figure 4f), which is consistent with the trends in energy consumption observed in the LTP/LTD measurements (Figure 3e). Thus, while ion transport determines the accuracy via its influence on G_{max}/G_{min}, hole transport, which is controlled by electrostatic gating, defines the energy consumption. This role division, which is enabled by the spatial separation of the ionic and electronic transport pathways, provides clear experimental evidence of accuracy-energy decoupling.

We estimated the $E_{p,image}$ values of previously reported systems to benchmark our device against grain boundary-mediated memtransistors. As the $E_{p,image}$ values were not directly reported in earlier studies, we reproduced their LTP/LTD operating conditions, G_{max}/G_{min} values, and conductances within the same simulation framework and calculated E_{prog} values under identical assumptions (Figure 4g). The $H_xK_{1-x}GaSb_2$ memtransistor exhibits the lowest $E_{p,image}$ among those of the compared devices, indicating that it maintains a high recognition accuracy while minimizing energy consumption. These characteristics suggest that the energy advantage of the vdW memtransistor likely persists, even upon scaling to large crossbar arrays.

3 | Conclusion

In this study, we demonstrated that a III–V vdW memtransistor with a path-decoupled ionic-electronic transport architecture could simultaneously display a wide G_{max}/G_{min} and an ultralow energy consumption. The spatial separation of the ionic and electronic pathways, combined with gate-controlled conductance tuning, enabled the selective reduction of E_{prog} while preserving G_{max}/G_{min}. MNIST handwritten-digit classification further confirmed that this mechanism maintained a high accuracy, even as the energy consumption was markedly reduced, thus overcoming the accuracy-energy trade-off in the conventional RRAM devices.

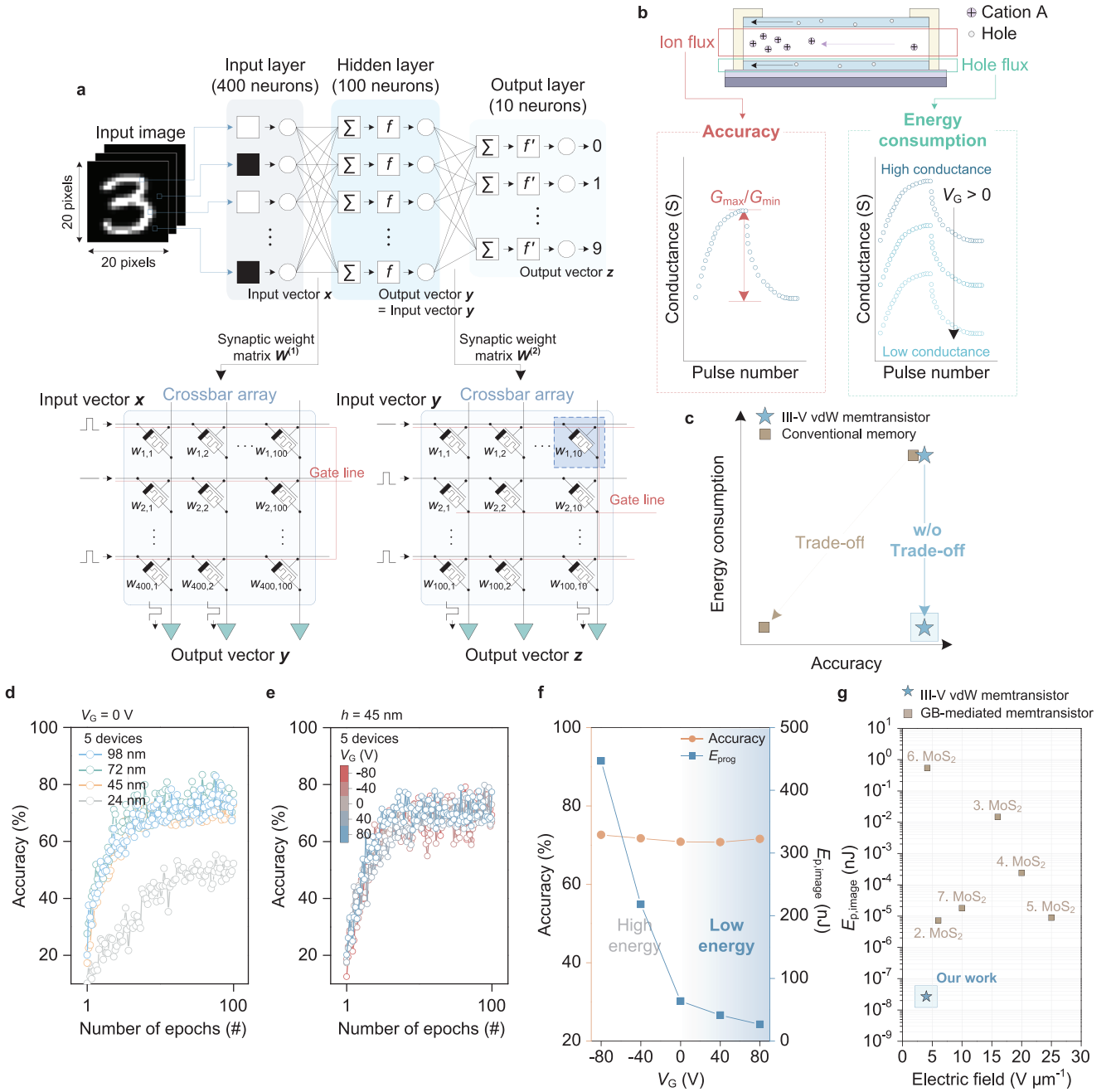

FIGURE 4 | Accuracy-energy decoupled MNIST handwritten-digit classification with path-decoupled memtransistor synapses. a) Schematic of the 400-100-10 multilayer perceptron used in simulation and its mapping onto crossbar arrays of $H_xK_{1-x}GaSb_2$ memtransistors. Each synaptic weight in the matrices $\boldsymbol{W}^{(1)}$ and $\boldsymbol{W}^{(2)}$ is represented by the conductance of a single device, such that an m × n crossbar implements an m × n weight matrix in parallel (400 × 100 and 100 × 10 for the first and second array, respectively). The gate lines tune the overall conductance. b) Derivation of accuracy-energy decoupling. The K^+ ion flux (L_{iq}) in the vdW gap sets G_{max}/G_{min} via Schottky barrier modulation (L_{qi}), thereby controlling synaptic weight resolution and recognition accuracy. In contrast, V_G tunes conductance (L_{qq}) in the III–V channel without changing G_{max}/G_{min}, thus setting energy consumption. c) Accuracy-energy diagram comparing conventional memristive devices and the III–V vdW memtransistor. A conventional memristive device displays an accuracy-energy trade-off, whereas the III–V vdW memtransistor realizes a high accuracy at a low energy by decoupling the ion and hole transport paths. d) Learning curves of devices with different h values (24, 45, 72, and 98 nm), derived from five devices for each condition. e) Recognition accuracy as a function of the number of training epochs using a 45-nm-thick device, with V_G varied from −80 to 80 V in steps of 40 V, each obtained from five devices. f) Programming energy per image ($E_{p,image}$) and recognition accuracy as functions of V_G. Whereas the accuracy remains almost constant, $E_{p,image}$ decreases by more than an order of magnitude as V_G increases, indicating accuracy-energy decoupling enabled by the path-decoupled ionic-electronic transport within the III–V vdW memtransistor. g) $E_{p,image}$ values of the $H_xK_{1-x}GaSb_2$ and previously reported grain boundary-mediated memtransistors. $H_xK_{1-x}GaSb_2$ memtransistor exhibits a lower $E_{p,image}$ than that of the grain boundary-mediated memtransistors.

The remaining challenges include improving the update linearity, shortening the channel for operation at an even lower energy, and developing scalable fabrication routes for producing large-area arrays. Nonetheless, the III–V vdW memtransistor introduces a novel material paradigm for energy-efficient neuromorphic hardware, which is rooted in its distinctive hybrid ionic-electronic transport functionality.

4 | Experimental Section

4.1 | Synthesis of the $KGaSb_2$ Crystals

Elemental K (0.4 g, 99% trace-metal basis, Sigma-Aldrich, St. Louis, MO, USA), Ga (0.6 g, 99.999% trace-metal basis, Sigma-Aldrich), and Sb beads (2.0 g; 99.999% trace-metal basis, Sigma-Aldrich) were combined in a stoichiometric ratio to produce $KGaSb_2$. Under Ar in a glovebox, 2 g of the premixed charge was loaded into an Al_2O_3 crucible and enclosed in a quartz double ampule. The ampule was removed from the glovebox and flame-sealed to prevent oxidation and mitigate K-induced quartz corrosion. The sealed assembly was heated to 750°C at 250°C h^{-1} and maintained for 40 h to melt and homogenize the reaction mixture. Slow cooling from 750 to 500°C over 100 h was then applied, followed by an isothermal hold at 500°C for 100 h to form $KGaSb_2$ crystals. The ampule was subsequently cooled to room temperature at 100°C h^{-1}, and then plate-like, silver-colored $KGaSb_2$ crystals (lateral sizes: 2–3 mm) were mechanically separated from the crucible inside the glovebox.

4.2 | Topochemical Approach to Prepare $H_xK_{1-x}GaSb_2$

Before etching, $GaCl_3$ (99.999%, Thermo Fisher Scientific, Waltham, MA, USA) was exposed to ambient humidity to form an aqueous $GaCl_3$ solution. $KGaSb_2$ powder (0.05 g) was immersed in the aqueous $GaCl_3$ at 50°C for 6 h to induce the topochemical reaction, yielding $H_xK_{1-x}GaSb_2$. The product was removed and rinsed sequentially: anhydrous ethylene glycol (99.8%, Sigma-Aldrich) was used to dissolve the KCl byproduct, and methanol was then used to displace the residual ethylene glycol. The solid was dried under vacuum for 24 h to afford black $H_xK_{1-x}GaSb_2$ powder.

4.3 | Memtransistor Device Fabrication

$H_xK_{1-x}GaSb_2$ crystals were mechanically exfoliated with adhesive tape inside an Ar-filled glovebox and transferred onto 300 nm insulating SiO_2/p^{++}-doped Si substrates. A photoresist (polymethyl methacrylate 5) film was then spin-coated, and source/drain electrodes were defined using electron-beam lithography. Au (total thickness: 100 nm), which was employed because the alignment of its work function with that of $H_xK_{1-x}GaSb_2$ led to a Schottky junction, was deposited via thermal evaporation, followed by sputtering. The p^{++}-doped Si served as the global bottom gate. Lift-off was conducted in acetone, and electrical characterization was performed at room temperature under ambient conditions using a 4200A-SCS semiconductor parameter system (Keithley Instruments, Cleveland, OH, USA).

4.4 | Calculation of the Programming Energy

The programming energy (E_{prog}) required for a single weight update in a three-terminal synaptic device can be estimated as $E_{prog} = V_{D,pulse}I_D\Delta t_w + V_GI_Gt_G$. $V_{D,pulse}$, V_G, I_D, I_G, Δt_w, and t_G represent the amplitudes of the drain voltage pulses, gate voltage, current during the $V_{D,pulse}$, gate leakage current, pulse width and duration time of applied V_G, respectively [49–51]. Here, E_{prog} denotes the device-level electrical energy dissipated during programming, determined by the channel conductance, and is distinct from the intrinsic ionic switching energy associated with ion migration and memory-state formation. In our synaptic memtransistor, the contribution from the gate term is negligible because I_G is extremely small; therefore, E_{prog} is dominated by the drain-side component.

4.5 | MNIST Handwritten-Digit Classification

Neural-network simulation was performed using the MLP+NeuroSim framework [52] and a 400-100-10 multilayer perceptron driven by 20 × 20 MNIST handwritten-digit images. Synaptic weights were mapped onto 16 × 16 memtransistor crossbar subarrays (256 devices per subarray), and the full network was implemented using a subarray-based array architecture to emulate the organization of physical hardware. We trained using one million examples randomly drawn from the 60 000-image training pool and evaluated the recognition accuracy using a disjoint 10 000-image test set. Each pixel fed an input neuron, and a sigmoid nonlinearity produced the network response. Synaptic weights were tied to device conductance such that the update magnitude followed the conductance increment (ΔG), with stochastic gradient ascent/descent using a delta-rule error. The device dynamics parameterizing the nonlinear learning rule were modeled as single-exponential functions of the pulse number N: the conductance during LTP and LTD were given by $G_{LTP} = B(1 - \exp(-N/A)) + G_{min}$ and $G_{LTD} = -B(1 - \exp[(N - N_{max})/A]) + G_{max}$, with $B = (G_{max} - G_{min})/(1 - \exp(-N_{max}/A))$, where G_{LTP} and G_{LTD} are the conductance for LTP and LTD, respectively. G_{max}, G_{min}, and N_{max} are extracted from experimental data. The recognition accuracy was computed every 10 000 training images, with the reported value given by the mean of the last ten recorded accuracy points. The recognition accuracy obtained from simulations with varying V_G is presented as the mean ± standard deviation.

Author Contributions

J.B., J.H.H., and W.S. designed the experiments. J.B., Taeyoung Kim, and J.W. synthesized the materials. J.B., S.P., and G.W.K. fabricated the devices and performed the measurements. J.B., S.K., H.C., and Taehoon Kim analyzed the electrical characteristics. H.-S.L., J.-H.L., Y.J.C., and J.C. contributed to the discussions. All authors contributed to the manuscript.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supporting Information

Additional supporting information can be found online in the Supporting Information section.

Supporting File: adma73350-sup-0001-SuppMat.docx.